Unleashing the Power of Parallel Compute!

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Agenda

- Radeon 5xxx Product Family Highlights
- Radeon 5870 vs. 4870
- Radeon 5870 Top-Level
- Radeon 5870 Shader Core
- References / Links / Screenshots
- Questions?
## ATI Radeon™ HD 5000 Series of GPU (Evergreen)

<table>
<thead>
<tr>
<th>Model</th>
<th>Process/Transistors</th>
<th>Stream Processors</th>
<th>Peak SP Flop Rate</th>
<th>Peak DP Flop Rate</th>
<th>Texel Rate</th>
<th>Pixel Rate</th>
<th>Max Resolution</th>
<th>Max Bandwidth</th>
<th>Max/Idle Board Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>5870 (Cypress)</td>
<td>40nm/2.15B</td>
<td>1600</td>
<td>2.72 Teraflops</td>
<td>544 GFLOPS</td>
<td>68 Gtex/sec</td>
<td>27.2 Gpix/sec</td>
<td>6x2560x1600</td>
<td>153 GB/s</td>
<td>188W/27 W</td>
</tr>
<tr>
<td>5770 (Juniper)</td>
<td>40nm/1.04B</td>
<td>800</td>
<td>1.36 Teraflops</td>
<td>34 Gtx/sec</td>
<td>34 Gtx/sec</td>
<td>13.6 Gpix/sec</td>
<td>6x2560x1600</td>
<td>77 GB/s</td>
<td>108W/18 W</td>
</tr>
<tr>
<td>5670 (Redwood)</td>
<td>40nm/627M</td>
<td>400</td>
<td>620 GFLOPS</td>
<td>15.5 Gtx/sec</td>
<td>6 Gtx/sec</td>
<td>6.2 Gpix/sec</td>
<td>4x2560x1600</td>
<td>64 GB/s</td>
<td>61W/14 W</td>
</tr>
<tr>
<td>5470 (Cedar)</td>
<td>40nm/292M</td>
<td>80</td>
<td>120 GFLOPS</td>
<td>3 Gtx/sec</td>
<td>3 Gtx/sec</td>
<td>64 GB/s</td>
<td>13-15W</td>
<td>26 GB/s</td>
<td>13-15W</td>
</tr>
</tbody>
</table>
## ATI Radeon™ HD 5870 GPU vs. 4870

<table>
<thead>
<tr>
<th></th>
<th>ATI Radeon™ HD 4870</th>
<th>ATI Radeon™ HD 5870</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>263 mm(^2)</td>
<td>334 mm(^2)</td>
<td>1.27x</td>
</tr>
<tr>
<td>Transistors</td>
<td>956 million</td>
<td>2.15 billion</td>
<td>2.25x</td>
</tr>
<tr>
<td>Memory Bandwidth</td>
<td>115 GB/sec</td>
<td>153 GB/sec</td>
<td>1.33x</td>
</tr>
<tr>
<td>L2-L1 Rd Bandwidth</td>
<td>512 bytes/clk</td>
<td>512 bytes/clk</td>
<td>1x</td>
</tr>
<tr>
<td>L1 Bandwidth</td>
<td>640 bytes/clk</td>
<td>1280 bytes/clk</td>
<td>2x</td>
</tr>
<tr>
<td>Vector GPR</td>
<td>2.62 Mbytes</td>
<td>5.24 MByte</td>
<td>2x</td>
</tr>
<tr>
<td>LDS Memory</td>
<td>160 kb</td>
<td>640kb</td>
<td>4x</td>
</tr>
<tr>
<td>LDS Bandwidth</td>
<td>640 byte/clk</td>
<td>2560 bytes/clk</td>
<td>4x</td>
</tr>
<tr>
<td>Concurrent Threads</td>
<td>15872</td>
<td>31744</td>
<td>2x</td>
</tr>
<tr>
<td>Shader (ALU units)</td>
<td>800</td>
<td>1600</td>
<td>2x</td>
</tr>
<tr>
<td>Board Power*</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Idle</td>
<td>90 W</td>
<td>27 W</td>
<td>0.3x</td>
</tr>
<tr>
<td>Max</td>
<td>160 W</td>
<td>188 W</td>
<td>1.17x</td>
</tr>
</tbody>
</table>

### Updated APIs
- dx11 w/ CS 5.0 – Shader Model 5.0
- OpenCL 1.1
- OpenGL 4.0
Unleashing the Power of Parallel Compute with AMD Stream Technology

June 2010
Double the processing power of previous generation
- 2.72 Teraflops
- 27.2 Giga Pixels/sec
“Dual” Unified Shader Engine
- I$/K$ for each SE
- Rasterizer per SE
- 248 concurrent wavefronts per SE
- 16 pixel ROP units per SE
Non-PS round-robin SE
PS, Screen-sub-divide
Dispatch Controller Prog
- can group PS waves
- cap a shader stage’s inflight wavefronts
Compute Aspects of ATI Radeon™ HD 5870

• SIMD Engine
  – Stream Cores
  – Local Data Share (LDS)
• Load / Store / Atomic Data Access
• Dispatch / Indirect Dispatch
• Global Data Share (GDS)
SIMD Engine

- SIMD Engine can process Wavefronts from multiple kernels concurrently.
- Thread divergence within a Wavefront is enabled with Lane Masking and Branching.
  - Enabling each Thread in a Wavefront to traverse a unique program execution path.
- Full hardware barrier support for up to 8 Work Groups per SIMD Engine (for thread data sharing).
- Each Stream Core receives up to the following per VLIW instruction issue:
  - 5 unique ALU Ops - or - 4 unique ALU Ops with a LDS Op (Up to 3 operands per thread).
- LDS and Global Memory access for byte, ubyte, short, ushort reads/writes supported at 32bit dword rates.
- Private Loads and read only texture reads via Read Cache.
- Unordered shared consistent loads/stores/atomics via R/W Cache.
- Wavefront length of 64 threads where each thread executes a 5 way VLIW Instruction each issue.
  - \( \frac{1}{4} \) Wavelength (16 threads) on each clock of 4 clocks (T0-15, T16-31, T32-47, T48-T63).
Stream Core with Processing Elements (PE)

Each Stream Core Unit includes:
- 4 PE
  - 4 Independent SP or Integer Ops
- 2 DP add or dependant SP pairs
- 1 DP fma or mult or SP dp4
- 1 Special Function PE
  - 1 SP or Integer Operation
  - SP or DP Transcendental Ops
- Operand Prep logic
- General Purpose Registers
- Data forwarding and predication logic
Processing Element (PE) Precision Improvements

- **FMA** (Fused Multiply Add), IEEE 754-2008 precise with all round modes, proper handling of Nan/Inf/Zero and full de-normal support in hardware for SP and DP

- **MULADD** instruction without truncation, enabling a $\text{MUL}_{\text{ieee}}$ followed $\text{ADD}_{\text{ieee}}$ to be combined with round and normalization after both multiplication and subsequent addition.

- **IEEE Rounding Modes** (Round to nearest even, Round toward +Infinity, Round toward –Infinity, Round toward zero) supported under program control anywhere in the shader. Double and single precision modes are controlled separately. Applies to all slots in a VLIW.

- **De-normal Programmable Mode** control for SP and DP independently. Separate control for input flush to zero and underflow flush to zero.

- **FP Conversion Ops** between 16 bit, 32 bit, and 64 bit floats with full IEEE 754 precision.

- **Exceptions Detection** in hardware for floating point numbers with software recording and reporting mechanism. Inexact, Underflow, Overflow, division by zero, de-normal, invalid operation
Processing Element (PE) Improved IPC

- Co-issue of dependant Ops in “ONE VLIW” instruction
  - full IEEE intermediate rounding & normalization
  - Dot4 \( (A=A*B + C*D + E*F + G*H) \)
  - Dual Dot2 \( (A = A*B + C*D; \quad F = G*h + I*J) \)
  - Dual Dependant Multiplies \( (A = A * B * C; \quad F = G * H * I;) \)
  - Dual Dependant Adds \( (A = B + C + D; \quad E = F + G + H;) \)
  - Dependant Muladd \( (A = A*B+C + D*E; \quad F = G*H + I + J*K) \)

- 24 bit integer
  - MUL, MULADD (4 – co-issue)
  - Heavy use for Integer thread group address calculation
Processing Element (PE) New Integer Ops

- 32b operand Count Bits Set
- 64b operand Count Bits Set
- Insert Bit field
- Extract Bit Field
- Find first Bit (high, low, signed high)
- Reverse bits
- Extended Integer Math
  - Integer Add with carry
  - Integer Subtract with borrow
- 1 bit pre-fix sum on 64b mask. (useful for compaction)
- Shader Accessible 64 bit counter
- Uniform indexing of constants
Processing Element (PE) Special Ops

- Conversion Ops
  - FP32 to FP64 and FP64 to FP32 (w/IEEE conversion rules)
  - FP32 to FP16 and FP 16 to FP32 (w/IEEE conversion rules)
  - FP32 to Int/UInt and Uint/Int to FP32
- Very Fast 8 bit Sum of Absolute Differences (SAD)
  - 4x1 SAD per lane, with 4x4 8 bit SAD in one VLIW
  - Used for video encoding, computer vision
  - Will be exposed via OpenCL extension
- Video Ops
  - 8 bit packed to float and float to 8 bit packed conversion Ops
  - 4 8 bit pixel average (bilinear interpolation with programmable round)
  - Arbitrary Byte or Bit extraction from 64 bits
Local Data Share (LDS)

Share Data between Work Items of a Work Group designed to increase performance

• High Bandwidth access per SIMD Engine (1024b/clk) – Peak is double external R/W bandwidth (512b/clk)
• Low Latency Access per SIMD Engine
  • 0 latency direct reads (Conflict free or Broadcast)
  • 1 VLIW instruction latency for LDS indirect Op
• All bank conflicts are hardware detected and serialized as necessary with fast support for broadcast reads
• Hardware allocation of LDS space per thread group dispatch
  • Base and size stored with wavefront for private access
• 32 – byte, ubyte, short, ushort reads/writes per clk (reads are sign extended)
• 32 dwords access per clock
  • Load/Stores
  • Atomics: add, sub, inc, dec, min, max, and, or, xor, exchange, compare _swap
  • Return pre-Op value to Stream Core 4 primary Processing Elements
Global Data Share (GDS)

- Similar to LDS except it is shared memory for entire dispatch (grid) as opposed to a work-group
- Low Latency Access to a global data shared memory between all threads in a kernel
  - 25 clks latency
  - Issued in parallel to math similar to fetch, return to GPR
- Why GDS vs. using regular global memory?
  - Large number of threads going at small amount of memory (ex. append counters, reduction) can create choke point, and under utilization of the hardware
  - Separate memory (GDS) for small shared allocation, can free up global memory for use by the shader sequencer for other wave-fronts
  - GDS is parallel to global memory
- Counters for append buffers here, and supports “Ordered” append as well
  - The append buffer is built in dispatch order
Global Data Share (GDS)

Dual Array of SIMD Engines

Global Data Share (GDS)
64 kb, 32 banks with Integer Atomic Units
References

Links to AMD’s OpenCL tutorial and some samples

AMD Developers Central : Samples, Tools, Downloads, White papers etc.
http://developer.amd.com/gpu/ATIStreamSDK/Pages/default.aspx

Khronos Open CL : Specification, Introduction Slides, and Quick Reference
www.khronos.org/opencl/

Direct Compute Introduction
Order-independent transparency (OIT)

DirectX® 11 Depth of Field in Action
Summary

ATI Stream™: Age of Teraflop Processing

Leadership in performance, power and price

Open software strategy based on standards

Compliant DirectX® 11 Direct Compute & OpenCl 1.1

Available Today in Stores!!
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