Memory Sharing and The Compute Architecture of Intel® Processor Graphics Gen8

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Agenda

• Introduction

• **Compute architecture:**
  - Execution units
  - Subslices, slices, products
  - Chip level architecture

• **Memory:**
  • Shared physical memory
  • Shared virtual memory & coherency
  • Application examples

• Summary
Intel® Processor Graphics?

- Intel® Processor Graphics: 3D Rendering, Media, and Compute

- Discrete class performance but... integrated on-die for true heterogeneous computing, SoC power efficiency, and a fully connected system architecture

- Some products are near TFLOPS performance

- The foundation is a highly threaded, data parallel compute architecture

- Today: focus on compute components of Intel Processor Graphics Gen8

Intel® Core™ i5 with Iris graphics 6100:

Intel Processor Graphics is a key Compute Resource
## Processor Graphics is a Key Intel Silicon Component

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<tr>
<th>Processor graphics gen6</th>
<th>Processor graphics gen7</th>
<th>Processor graphics gen7.5</th>
<th>Processor graphics gen8</th>
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Example OEM Products with Processor Graphics

- Apple® Macbook® Pro 15"
- Apple® Macbook Pro 13"
- Apple iMac® 21.5"
- Gigabyte® Brix® Pro
- Sony® Vaio® Tap 21
- Microsoft® Surface® Pro 3
- Toshiba® Encore® 2 Tablet
- Asus® Transformer Pad
- Lenovo® Miix® 2
- Asus Zenbook Infinity®
- Zotac® ZBOX® EI730
- JD.com – Terran Force
- Clevo® Niagara®

The Graphics Architecture for many OEM DT, LT, 2:1, tablet products
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• Summary
EU: Multi-threaded execution

- 7 HW threads, 4K register file each
- Combination of **SMT** & **IMT**
  - Thread Arbiter picks instructions to run from runnable thread(s)
- Dispatches instruction to appropriate functional unit
- Each cycle: can co-issue multiple instructions, from up to four different threads
- Each thread executes a unique kernel
  - Different instances of same src kernel
  - Different src or new kernels

SMT – Simultaneous Multi-.Threading
IMT – Interleaved Multi-Threading
**EU: Instructions & FPUs**

1. **Instructions:**
   - 2 or 3 src registers, 1 dst register
   - Instructions are *variable width SIMD*.
   - Logically programmable as 1, 2, 4, 8, 16, 32 wide SIMD
   - SIMD width can change back to back w/o penalty
   - Optimize register footprint, compute density

2. **2 Arithmetic, Logic, Floating-Pt Units**
   - *Physically* 4-wide SIMD, 32-bit lanes

3. **Min FPU instruction latency is 2 clocks**
   - SIMD-1, 2, 4, 8 float ops: 2 clocks
   - SIMD-16 float ops: 4 clocks
   - SIMD-32 float ops: 8 clocks

FPUs are fully pipelined across threads: instructions complete every cycle.
EU: Universal I/O Messages

The Messaging Unit

1. **Send** is the universal I/O instruction

2. Many send message types:
   - Mem stores/reads are messages
   - Mem scatter/gathers are messages
   - Texture Sampling is a message with u,v,w coordinates per SIMD lane
   - Messages used for synchronization, atomic operations, fences etc.
Subslice: An Array of 8 EU's

Each: Subslice

① Eight Execution Units

② Local Thread Dispatcher & Inst $\$

③ Texture/Image Sampler Unit:
  • Includes dedicated L1 & L2 caches
  • Dedicated logic for dynamic texture decompression, texel filtering, texel addressing modes
  • 64 Bytes/cycle read bandwidth

④ Data Port:
  • General purpose load/store S/G Mem unit
  • Memory request coalescence
  • 64 Bytes/cycle read & write bandwidth
Slice: 3x Subslices

Each Slice: 3 x 8 = 24 EU’s
- 3x8x7 = 168 HW threads
- 3x8x7xSIMD32 = 5376 kernel insts

1. Dedicated interface for every sampler & data port

2. Level-3 (L3) Data Cache:
   - Typically 384 KB / slice in multiple banks, (allocation sizes are driver reconfigurable)
   - 64 byte cachelines
   - Monolithic, but distributed cache
   - 64 bytes/cycle read & write
   - Scalable fabric for larger designs

3. Shared Local Memory:
   - 64 KB / subslice
   - More highly banked than rest of L3

4. Hardware Barriers, 32bit atomics
Chip Level Architecture

- **Ring Interconnect:**
  - Dedicated “stops”: each CPU Core, Graphics, & System Agent
  - Bi-directional, 32 Bytes wide

- **Shared Last Level Cache (LLC):**
  - Both GPU & CPU cores
  - 2-8MB, depending on product
  - Inclusive

- **Optimized for CPU & GPU coherency:**
  - Address hashing to multiple concurrent LLC request queues
  - LLC avoids needless snoops “upwards”
Chip Level Architecture:
4 CPU cores & Iris Pro Graphics: 48 EUs, & EDRAM
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• Summary
Shared Physical Memory: a.k.a. Unified Memory Architecture (UMA)

• Long History: ...Gen2...Gen6, Gen7, Gen7.5, Gen8 all employed shared physical memory
• No need for additional GDDR memory package or controller. Conserves overall system memory footprint & system power
• Intel® Processor Graphics has full performance access to system memory
• “Zero Copy” CPU & Graphics data sharing
• Enabled by buffer allocation flags in OpenCL™, DirectX®, etc.

Shared Physical Memory means “Zero Copy” Sharing
Shared Virtual Memory

- Significant feature, new in Gen8
- Seamless sharing of pointer rich data-structures in a shared virtual address space
- Hardware-supported byte-level CPU & GPU coherency, cache snooping protocols...
- Spec'd Intel® VT-d IOMMU features enable heterogeneous virtual memory, shared page tables, page faulting.
- Facilitated by OpenCL™ 2.0 Shared Virtual Memory:
  - Coarse & fine grained SVM
  - CPU & GPU atomics as synchronization primitives
Mapping Memory Spaces to Memory Hierarchy

1. Cached memory hierarchy supporting global, constant, and image data
2. Shared (local) memory reads & writes
3. Image reads
4. Buffer & local reads & writes. Also image writes

- All memory caches are globally **coherent** (except for sampler & shared local memory)
- CPU & GPU sharing at full bandwidth of LLC
SVM: Cyberlink Photo Director’s “Clarify Effect”

- Concurrent CPU & GPU computes applied to a single coherent buffer
- Border pixels have different algorithm, conditional degrades GPU efficiency
- SVM Implementation:
  - CPU does border
  - GPU does interior, with no conditionals
  - Seamless, correct sharing, even when cachelines cross border regions
SVM: Behavior Driven Crowd Simulation (UNC collab)

- A sea of autonomous “agents” from start to goal positions. Complex collisions and interactions in transit. (Visualized here as pixels.)

- C pointer rich agent spatial dynamic data structure developed for multi-core CPU

- SVM Implementation:
  - Ported quickly to GPU and SVM buffers without data-structure re-write
  - Enables both GPU & multiple CPU to concurrently support computation on single data-structure, plus GPU rendering

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Summary

- Intel® Processor Graphics: 3D Rendering, Media, and **Compute**
- Many products, APIs, & applications using Intel® Processor Graphics for compute
- **Gen8 Architecture:**
  - Execution Units, Slices, SubSlices, Many SoC product configs
  - Layered memory hierarchy founded shared LLC.
- Shared Physical Memory, Shared Virtual Memory
  - No separate discrete memory, No PCIe bus to GPU.
  - SVM & *real* GPU/CPU cache coherency is here: use it, join us.
- Hint: See more at Intel Developer Forum in 1 week (Aug 18th, 2015)
Backup
EU: The Execution Unit

1. Gen8: Seven hardware threads per EU
2. 128 “GRF” registers per thread
   - 4K registers/thread or 28K/EU
3. Each “GRF” register:
   - 32 bytes wide
     - Eight: 32b floats or 32b integers
     - Sixteen: 16b half-floats or 16b shorts
   - Byte addressable
4. Architecture Registers per thread:
   - Program Counters
   - Accumulators
   - Index & predicate registers
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